CLAIMS

We claim:

1. A circuit for biasing an amplifier transistor comprising a control terminal, a current-sink terminal, and a current-source terminal, the circuit comprising:

a bias transistor including a control terminal, current-sink terminal, and a current-source terminal;

a first DC input port connected to the current sink terminal of the bias transistor;

a first resonator element operatively coupled to the current-sink terminal of the bias transistor and ground;

a second DC input port connected to the control terminal of the bias transistor;

a diode element operatively coupled to the control terminal of the bias transistor and ground;

a second resonator element operatively coupled to the control terminal of the bias transistor and ground; and

a resistive element operatively coupled to the current source terminal of the bias transistor and the control terminal of the amplifier transistor.

2. The circuit as set forth in claim 1 wherein the bias transistor is one of a BJT, an HBT and a FET.

3. The circuit as set forth in claim 1 wherein the amplifier transistor is one of a BJT, an HBT and a FET.

4. The circuit as set forth in claim 1 wherein the first resonator is an RLC circuit.

5. The circuit as set forth in claim 1 wherein the diode element comprises a plurality of diodes.

6. The circuit as set forth in claim 1 wherein the second resonator is an RLC circuit.

7. The circuit as set forth in claim 1 wherein the resistive element is a resistor.

8. The circuit as set forth in claim 1 wherein the resistive element is an RLC circuit.

9. The circuit as set forth in claim 8 wherein the resistive element further comprises a resistor.

10. A circuit for biasing an amplifier transistor including a control terminal, current-sink terminal, and current-source terminal wherein the circuit is suitably adapted to utilize a bias circuitry surrounding the amplifier transistor to provide intermodulation cancellation and dynamic power control, the circuit comprising:

means for applying an original input signal to an input port;

means for controlling flow of a leakage signal of the original input signal into the bias circuitry;

means for altering the electrical characteristics of the leakage signal to create an altered input signal; and

means for applying the altered input signal to the base of the amplifier transistor.

11. The circuit set forth in claim 10 wherein the original input signal is an RF input signal.

12. The circuit as set forth in claim 10 wherein the means for controlling the flow of the leakage current is a resistive element.

13. The circuit as set forth in claim 10 wherein the means for controlling the flow of leakage current is an RLC circuit.

14. The circuit as set forth in claim 10 wherein the means for altering the electrical characteristics of the leakage signal includes resonator elements to control the impedance and shifting bias within the bias circuitry to reduce intermodulation distortion in the leakage signal.

15. The circuit as set forth in claim 10 further comprising means for canceling distortion in the leakage signal.

16. A method, comprising:

applying an original signal;

regulating a flow of a leakage signal of the original signal to a bias circuit;

controlling an impedance of the bias circuit to cancel intermodulation of the leakage signal;

creating an altered signal by shifting a bias point of the leakage signal;

combining the original signal and the altered signal; and

amplifying the combined signal.